Count/Store Assembly (638-6063-001)

Rockwell International

instructions

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1. DESCRIPTION

The Count/Store Assembly 638-6063-001, shown in figure 1, is a two-layer circuit board using a ribbon-type cable connector. The count/store assembly consists of the following functional circuits: 500- to 600-Hz oscillator, divide-by-64 divider, frequency change rate counter, frequency change rate storage register, dial lock circuit, and an up/down change control.

(To Be Supplied)

Count/Store Assembly
Figure 1

1.1 Optical Tuning Switch Assembly (610-2150-001)

The Optical Tuning Switch Assembly, Collins part number 610-2150-001, shown in figure 2, contains two boards, a lens ring, and a control knob. The emitter board contains a photoemissive device, the detector board contains a photosensitive device, and a lens ring coupled to the control knob separates the two boards. The detector board contains two clock generators to develop an up/down signal and a rate change signal.

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 3.)

The count/store assembly receives two clock signals which are frequency direction phase-shifted, a local enable input, a dial lock input, and a clock inhibit input; and provides fire bcd rate control outputs and an up/down signal output.

(To Be Supplied)

The optical tuning switch assembly provides two output clock signals. The directional that the control knob (front-panel TUNING knob) is tuned determines the phase-relationship of the clock signals.

Optical Tuning Switch Assembly
Figure 2

2.2 Up/Down Control

When the front-panel TUNING knob is tuned in a clockwise direction, clock B leads clock A; thus, clock B is positive when the positive going edge of clock A appears. U6A is set by the logic 1 at U6A-D when U6A is clocked and provides a logic 1 up/$\overline{\text{down}}$ (up) signal to U4-D2.

When the front-panel TUNING knob is turned in a counterclockwise direction, clock A leads clock B; thus, clock B is negative when the positive going edge of clock A appears. U6A is reset by the logic 0 at U6A-$\overline{\text{D}}$ when U6A is clocked and provides a logic 0 up/$\overline{\text{down}}$ (down) signal to U4-D2.

2.3 Rate Control

Rate control outputs are controlled by the frequency with which clock A pulses are applied to the count/store assembly. Clock A pulses are supplied through clock gate U11D, count/store inhibit gate U10C, and applied to the oscillator/clock-window circuit. Clock-window gate U11B is enabled at an 8- to 10-Hz rate with a 100- to 120-ms pulse. During the elapsed time (100 to 120 ms) of the clock window, the rate counter U2 counts the number of clock pulses until the clock window is removed. The output of counter is coupled through storage register U3/U4 to the rate outputs.

The rate that pulses can be applied using the optical tuning switch assembly is 0 to approximately 270 Hz. (There are 90 pulses applied per rotation of the control knob, and maximum rotation speed is approximately 3 turns per second.)

Clock gate U11D provides an output pulse only when a logic 1 input is first applied. If a steady logic 1 or logic 0 input was applied, the output of U11D would go to logic 1 after the RC time constant of R1-C1 had elapsed. This device causes a logic 1 output to be supplied from U11D with any fixed logic level input.

Count/store inhibit gate U10C prevents clock pulses from being applied if: (1) +5-V dc power has just been applied, (2) +5- and +15-V dc power is $\overline{\text{up to power}}$, (3) a $\overline{\text{dial lock}}$ signal is applied, and (4) a $\overline{\text{clock inhibit}}$ signal is applied. When all of the preceding conditions are initiated, U10C is enabled and U3/U4 is enabled.

When U10C is enabled, clock pulses are supplied through U10C to U7D (rate window gate) and U11B (rate count gate).

In the inactive state (no clock pulses applied), the following conditions are set up in the rate window and rate count circuits. U9 count is latched; that is, count 64 at Q7 is logic 1 which inhibits counter oscillator gate U10A and prevents further counting of U9. U8D output is logic 0 which causes U10B output to go to logic 1, enabling U7D (rate window gate) to receive a clock pulse. The logic 0 U8D output also causes output of U10D to go to logic 1 setting U6B. The output of U6B goes to logic 0 and U7C goes to logic 1, enabling reset gate U1B. The logic 1 output of U10D also resets rate count of U2 to 0.

When clock pulse is applied to U7D, it is transferred through U7D and U1B and resets U9. The output at U9-Q7 goes to logic 0, and counter oscillator gate U10A is enabled; U9 is clocked (and counts) at a 500- to 650-Hz rate through 64 counts. While counter U9 is counting through 64, a clock window is developed by U8D and U11B which allows input clock pulses to be applied through U11B and U5C to U2. Up to 31 counts can be applied to U2 in this window before clock inhibit gate U5C is inhibited by AND gate circuit (U5D, U1A, U1C). When 64 clocks are received by rate window counter U9, the rate window and rate count circuits are reset and the count starts over from 0.

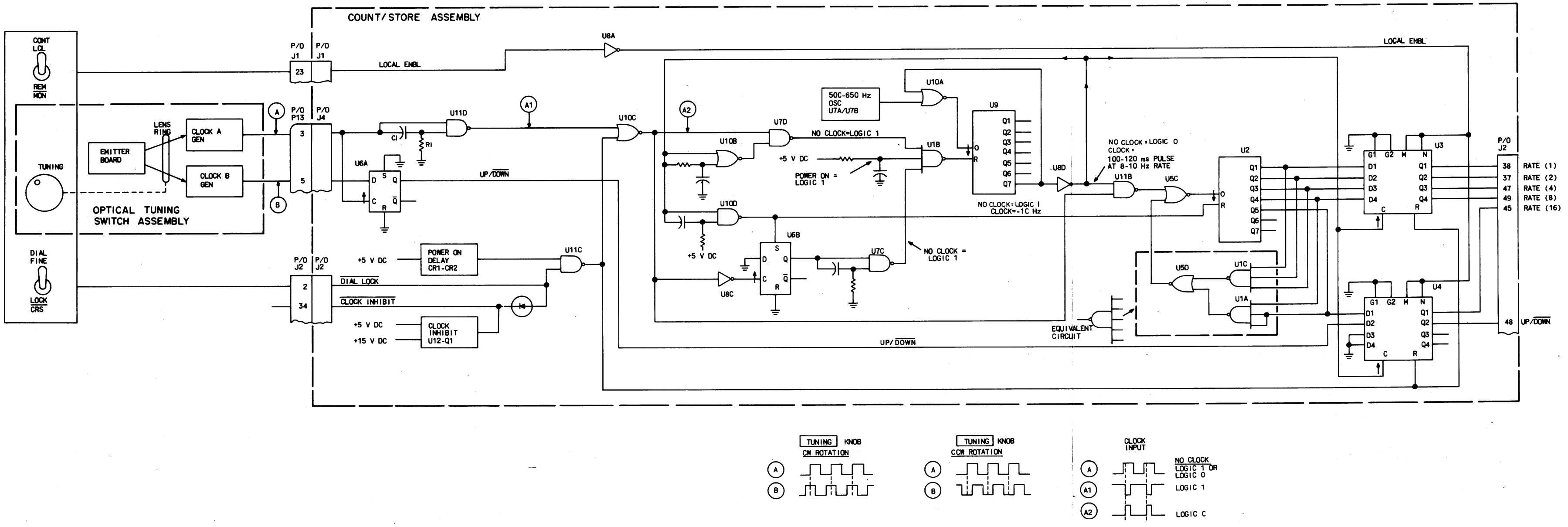
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test and troubleshoot the count/store assembly and the optical tuning switch assembly are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check the total performance of the count/store assembly. The test procedures in table 2 check the total performance of the optical tuning switch assembly. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



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Count/Store Assembly and Optical Tuning Switch Assembly, Block Diagram
Figure 3

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	***Note*** In these testing and troubleshooting procedures, two TTL logic level, square wave pulse train inputs to the count-store assembly (clock A and clock B) are required. The two pulse trains must be displaced by 90 ±20 degrees, with clock A lagging clock B for an up count, and clock A leading clock B for a down count. Circuits to generate the two square wave pulse trains may be incorporated into a test fixture so that only a single external pulse generator is required. a. Remove top and bottom cover of unit containing the count/store assembly that is to be tested. b. Disconnect P13 that connects count/store assembly J4 to optical tuning switch assembly. ***Note*** Upon completion of count/store assembly testing, reconnect P13 and J4. c. Set unit LINE SELECTOR for power source available (100/115/215/230 V ac). ***Note*** Ensure that proper fuse is installed for power source used. d. Connect unit to available power source.		
2. Initial checks	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw. b. Measure dc voltages between the following points and ground (TP1): J2-10 J2-16 J4-1	 +15 ±1.0 V dc. +5 ±0.5 V dc. +5 ±0.5 V dc.	 Check associated power supply.

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Count window oscillator	a. Front-panel controls set as follows: PWR to on. COUNT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Measure the count window oscillator frequency at U7B-4.	545 to 665 Hz	Check U7A, U7B, and associated circuit.
	d. Measure pulse width of count window at TP2.	120 to 100 ms.	Check U11D, U10C, U7D, U1B, U10A, U9, and associated circuits.
	e. Remove clock A and clock B inputs from J4-3 and J4-5.		
	f. Measure voltage level at TP2.	NLT +3.0 V dc.	Same as step 3.d.
4. Counter weight	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Vary the input clock frequency and measure the input frequency required to maintain a steady logic 1 (NLT +3.0 V dc) output on only one of each of the counter weight outputs.		If test 3 is okay, check U8D, U15B, U5C, U2, U3, U4, and associated circuits.
	J2-38 (rate 1) J2-37 (rate 2) J2-47 (rate 4) J2-49 (rate 8) J2-45 (rate 16)	33 to 45 Hz 67 to 83 Hz 135 to 165 Hz 270 to 330 Hz 540 to 660 Hz	

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Up/$\overline{\text{down}}$ direction	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw. b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down). c. Vary the phase of clock A and clock B, and measure the dc voltage at J2-48 (up/down).	Clock A leads clock B by 90; J2-48 = NMT +0.5 V dc. Clock A lags clock B by 90; J2-48 = NLT +3.0 V dc.	Check U6A, U4, and associated circuits.
6. $\overline{\text{Dial lock}}$	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw. b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz to J4-5 (clock B, up/down). c. Vary the phase of clock A and clock B, and measure the voltages at each rate output. J2-38 (rate 1) J2-37 (rate 2) J2-47 (rate 4) J2-49 (rate 8) J2-45 (rate 16) d. Set DIAL switch to FINE. e. Repeat step 4.c.	NMT 0.5 V dc Same as step 4.c.	Check U11C and associated circuits. Same as step 4.c.

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. Local/remote	a. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Measure input at U3-1, -2 and U4-1, -2.	NLT +3.0 V dc.	Check U8A and associated circuit.
	c. Set CONT switch to LCL.		
	d. Measure input at U3-1, -2, and U4-1, -2.	NMT 0.5 V dc.	Same as step 7.b.
8. Continuous/ single clock	a. Front-panel controls set as follows: PWR to on. CONT to LCL MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Connect clock A, set at 25 Hz, to J4-3 (clock A, count) and clock B, set at 25 Hz, to J4-5 (clock B, up/down).		
	c. Measure the pulses at TP3.	10- to 30-μs pulse width, 100 to 120 μs between pulses.	If test 3 and 4 are okay, check U5B and associated circuit.
	d. Remove clock A and block B inputs from J4-3 and J4-5.		
	e. Measure the pulses at TP3 while applying a single clock A pulse at J4-3.	Should be two pulses generated as indicated in step 8.c.	Same as step 8.c.
	f. Measure the rate 1 output at J2-38 while applying a single clock A pulse at J4-3.	Should go momentarily to logic 1 (NLT +3 V dc) then return to logic 0.	Same as test 4.
9. Power off check (Cont)	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		

Table 1. Count/Store Assembly, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	b. Measure dc voltage at J2-34 (clock inhibit) while momentarily setting PWR switch off and returning it on.	Goes to logic 0 (NMT 0.5 V dc) for 2 to 20 seconds after power is restored, then switches to logic 1 (NLT +3.0 V dc).	Check U12 and associated circuit.
10. Test complete	a. Set PWR switch off. b. Disconnect external power from rear panel. c. Remove test equipment from J4 and reconnect P13 to count/store assembly J4. d. Reinstall top cover of unit.		

Table 2. Optical Tuning Switch Assembly, Testing Procedures.

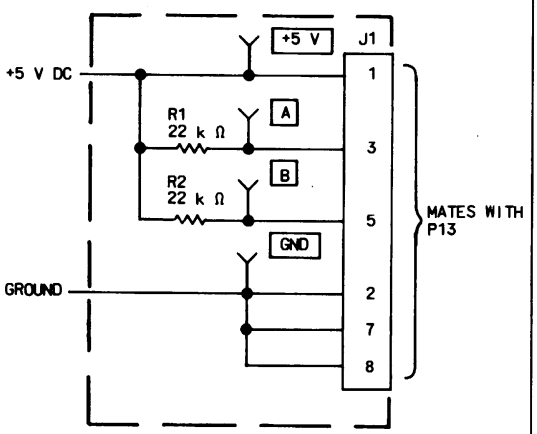
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top and bottom cover of unit containing the optical tuning switch assembly to be tested. b. Disconnect P13 that connects count/store assembly J4 to optical tuning switch assembly. ***Note*** Upon completion of optical tuning switch assembly testing reconnect P13 and J4. c. Connect the test jig shown below to P13. ***Note*** It is not necessary to apply power to the unit. 		If any abnormal indications occur in the optical tuning switch assembly, return it to the factory for repair.
2. Static state	With power applied check static state outputs of A and B.	Logic 1 or logic 0 are acceptable. Logic 1 = NLT +3 V dc. Logic 0 = NMT 0.5 V dc.	
3. TUNING knob rotation (Cont)	a. Connect a dual-trace oscilloscope to test jig: A to input A and trigger t, and B to input B. b. Note waveforms when rotating TUNING knob in a clockwise direction.	Waveform A lags Waveform B by 90 ±20 degrees.	

Table 2. Optical Tuning Switch Assembly, Testing Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	c. Note waveforms when rotating TUNING knob in a counterclockwise direction.	Waveform A leads waveform B by 90 ±20 degrees.	
4. Test complete	a. Remove test equipment from P13 and reconnect P13 to count/store assembly J4. b. Reinstall top cover of unit.		

4. REPAIR

Repair of the count/store assembly is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

Field repair of the optical tuning switch assembly is not recommended. If it fails, return it to the factory for service.

5. PARTS LIST/DIAGRAMS

This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 4). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

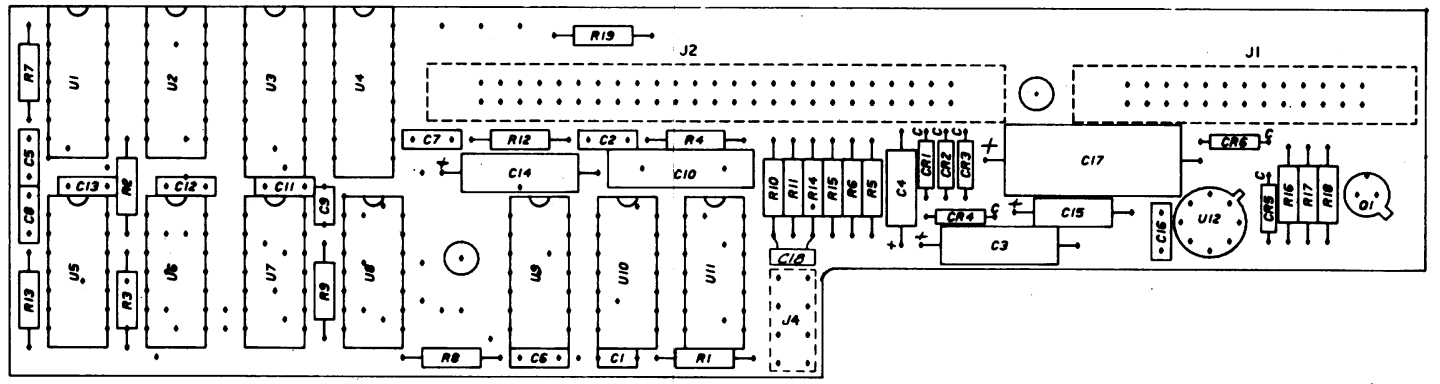
Use the reference designator indicated on the schematic and parts location diagram to locate part in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

A schematic diagram only (no parts list) is given for the optical tuning switch assembly (figure 5).

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Count/store assembly	638-6063-001	REV A
Optical tuning switch assembly	610-2150-001	REV —



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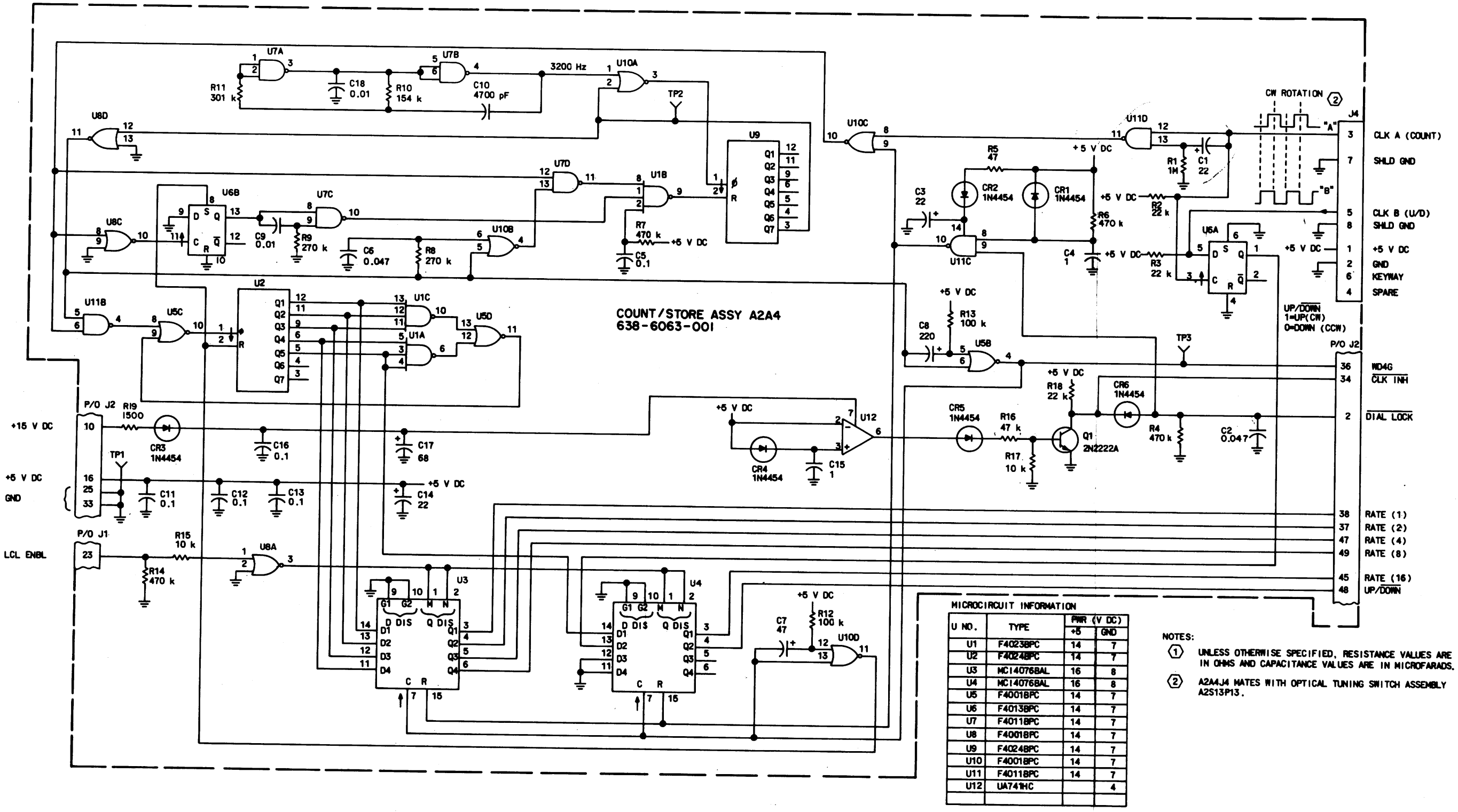
Count/Store Assembly, Schematic Diagram
Figure 4 (Sheet 1 of 3)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	COUNT/STORE ASSEMBLY	638-6063-001	
CR1-CR6	SEMICOND DEVICE 1N4454	353-3644-010	
C1	CAPACITOR,FXD CER DIEL, 22PF, 10%, 200V	913-5019-050	
C2	CAPACITOR,FXD CER DIEL, 0.047UF, 10%, 100V	913-5019-400	
C3	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C4	CAPACITOR,FXD ELCTLT, 1UF, 10%, 50V	184-9087-430	
C5	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C6	CAPACITOR,FXD CER DIEL, 0.047UF, 10%, 100V	913-5019-400	
C7	CAPACITOR,FXD CER DIEL, 47PF, 10%, 200V	913-4002-000	
C8	CAPACITOR,FXD CER DIEL, 220PF, 10%, 200V	913-4010-000	
C9	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C10	CAPACITOR,FXD MICA DIEL, 4700PF, 5%, 300V	912-3366-000	
C11-C13	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C14	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C15	CAPACITOR,FXD ELCTLT, 1UF, 10%, 50V	184-9087-430	
C16	CAPACITOR,FXD CER DIEL, 0.1UF, 10%, 100V	913-5019-440	
C17	CAPACITOR,FXD ELCTLT, 68UF, 10%, 20V	184-9086-580	
C18	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
Q1	TRANSISTOR 2N2222A	352-0661-020	
R1	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R2,R3	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W	745-0797-000	
R4	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R5	RESISTOR,FXD CMPSN, 47 OHMS, 10%, 1/4W	745-0701-000	
R6,R7	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R8,R9	RESISTOR,FXD CMPSN, 0.27MEGO, 10%, 1/4W	745-0836-000	
R10	RESISTOR,FXD FILM, 154K, 1%, 1/8W	705-1101-000	
R11	RESISTOR,FXD FILM, 301K, 1%, 1/8W	705-1115-000	
R12,R13	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R14	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R15	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R16	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R17	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R18	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W	745-0797-000	
R19	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/4W	745-0755-000	
U1	INTEGRATED CIRCUIT F4023BPC	351-8159-360	
U2	INTEGRATED CIRCUIT F4024BPC	351-8159-100	
U3,U4	INTEGRATED CIRCUIT MC14076BAL	351-8386-010	
U5	INTEGRATED CIRCUIT F4001BPC	351-8159-320	
U6	INTEGRATED CIRCUIT F4013BPC	351-8159-110	
U7	INTEGRATED CIRCUIT F4011BPC	351-8159-340	
U8	INTEGRATED CIRCUIT F4001BPC	351-8159-320	
U9	INTEGRATED CIRCUIT F4024BPC	351-8159-100	
U10	INTEGRATED CIRCUIT F4001BPC	351-8159-320	
U11	INTEGRATED CIRCUIT F4011BPC	351-8159-340	
U12	INTEGRATED CIRCUIT UA741HC	351-1029-010	

Count/Store Assembly, Schematic Diagram
Figure 4 (Sheet 2)



MICROCIRCUIT INFORMATION

U NO.	TYPE	PWR (V DC) +5	GND
U1	F40238PC	14	7
U2	F40248PC	14	7
U3	MC14076BAL	16	8
U4	MC14076BAL	16	8
U5	F40018PC	14	7
U6	F40138PC	14	7
U7	F40118PC	14	7
U8	F40018PC	14	7
U9	F40248PC	14	7
U10	F40018PC	14	7
U11	F40118PC	14	7
U12	UA741HC		4

NOTES:

(1) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

(2) A2A4J4 MATES WITH OPTICAL TUNING SWITCH ASSEMBLY A2S13P13.

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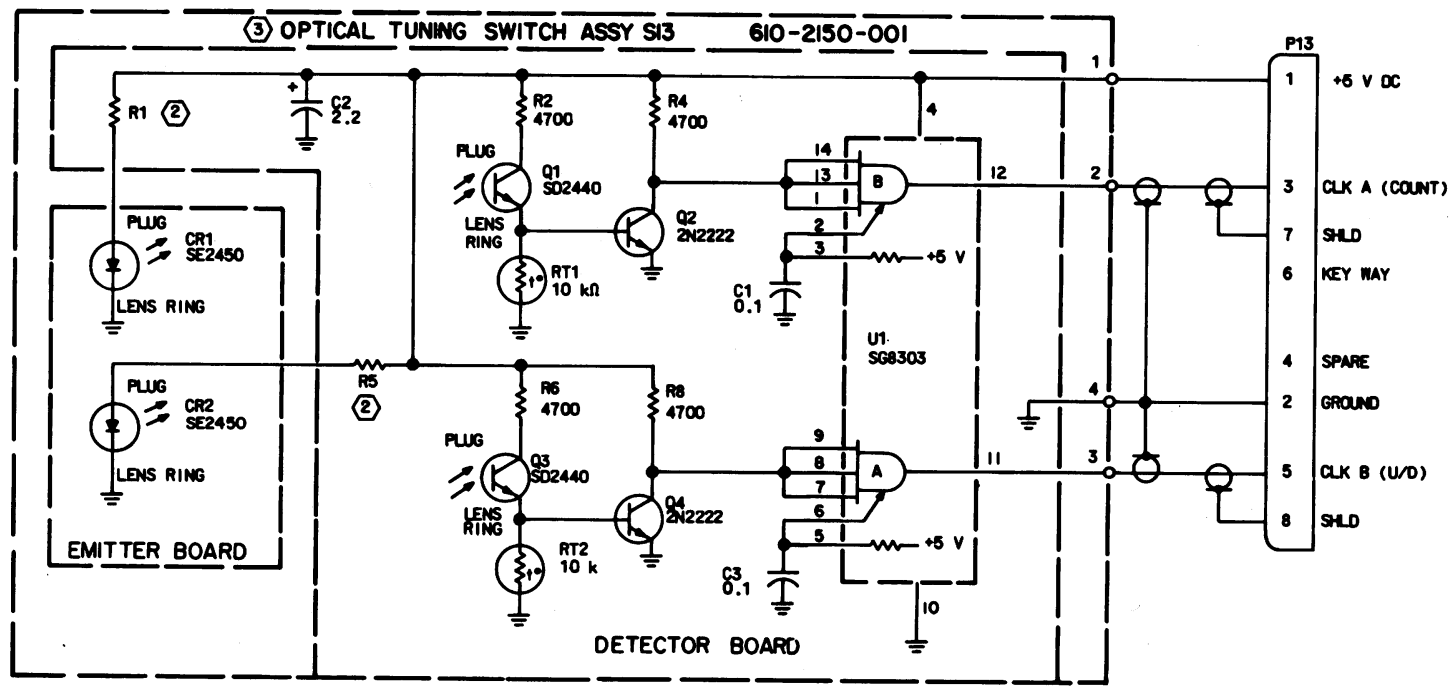
Count/Store Assembly, Schematic Diagram
Figure 4 (Sheet 3)



NOTES:

① UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

② VALUE SELECTED IN FINAL TEST.

③ FIELD REPAIR OF OPTICAL TUNING SWITCH ASSEMBLY IS NOT RECOMMENDED.

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Optical Tuning Switch Assembly, Schematic Diagram
Figure 5